REMARKS

Applicant, hereby, cancels claims 12 and 13 without prejudice or disclaimer. Therefore, claims 1, 3, 5-9 and 11 are all the claims pending in the application.

Claim objections

The Examiner maintains that in new claims 11-13, there is no antecedent basis for "the start up circuit means". In view of the amendments to claim 11 and cancellation of claims 12 and 13, Applicant requests the Examiner to withdraw the objection.

Rejection of claims 1, 5, 7, 9 and 11-13 under § 103(a) over Applicant's prior art Fig. 1 in view of Wu and Lee

Claims 1, 5, 7, 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. (5,307,007) and Lee (6,356,139). Applicant submits the following in traversal.

Claim 1

Without conceding on the patentability of unamended claim 1, Applicant amends claim 1 to recite the subject matter of claims 12 and 13. Applicant submits that features of claims 12 and 13 (now amended into claim 1) are not disclosed or suggested by Applicant's Prior Art Fig. 1 in view of Wu and Lee at least for the following reasons.

Claim 1 recites "a start up circuit means for improving stability characteristics of the constant bias voltage at a high frequency range and eliminating noise from the power source voltage". On the contrary, the combination of the Applicant's Prior Art Fig. 1, Wu and Lee merely discloses a start-up function. Applicant submits that the above noted features are not disclosed or suggested by the combination of the Applicant's Prior Art Fig. 1, Wu and Lee.

Additionally, the Examiner, in the current Office Action, alleges that the combination of the Applicant's Prior Art Fig. 1, Wu and Lee inherently possesses the properties recited in claims 12 and 13 (now amended into claim 1). Applicant submits that according to MPEP § 2112 ""In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)". Since the Examiner does not provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic of claims 12 and 13 (now amended into claim 1) necessarily flows from the teachings of the combination of the Applicant's Prior Art Fig. 1, Wu and Lee, Applicant submits that the above noted features of claim 1 are not disclosed or suggested by the combination of the Applicant's Prior Art Fig. 1, Wu and Lee.

In view of the foregoing, Applicant respectfully submits that claim 1 is patentable.

For reasons similar to those submitted for claim 1, Applicant respectfully submits that claim 9 is patentable.

Claims 5, 7 and 11, which depend from claim 1, are patentable at least by virtue of their dependencies.

Rejection of claims 3, 6 and 8 under § 103(a) over Applicant's prior art Fig. 1 in view of Wu and Park

Claims 3, 6 and 8 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. (5,307,007) and Park et al. (5,880,625). Applicant submits the following in traversal.

Claim 3

Applicant submits that claim 3 is patentable. In the Office Action dated July 9, 2009, the Examiner maintains that features of claim 3 are disclosed by the combination of the Applicant's prior art Fig. 1, Wu and Park. Specifically, the Examiner asserts that the Applicant's prior art Fig. 1 discloses a third PMOS transistor MP11, a fourth PMOS transistor MP12, a first NMOS transistor MN13, a second NMOS transistor MN 14 and a resistor R11. However, the Examiner concedes that the Applicant's prior art Fig. 1 does not show the first and second PMOS transistors as recited in claim 3, but cites Fig. 5 of Park to make up for the deficiency. In addition, the Examiner concedes that the alleged cascoded arrangement by combining the teachings of the Applicant's prior art Fig. 1 and Park does not disclose a first and second capacitor, as claimed in claim 3. The Examiner cites Fig. 3 (cascoded structure) of Wu to make up for the deficiency. Applicant disagrees with the Examiner for the following reasons.

Applicant notes that the first and second capacitors of the cascoded structure of Wu are connected between the gate junction M3/M4 and M5/M6 and the gate junction M5/M6 and M7/M8, respectively (see Fig. 3 of Wu). M3, M4, M5, M6, M7 and M8 are disclosed in Wu as NMOS transistors (col. 3, lines 31-36). On the other hand, it is noted that the Examiner alleges that a combination of the teachings of the Applicant's prior art Fig. 1 and Park yield 4 PMOS transistors and 2 NMOS transistors (see Fig. 5 of Park). The Examiner alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to connect a first capacitor as taught by Wu between the first common node (which the Examiner alleges as corresponding to the gate junction (PMOS) M53/M54 of Park) and the second common node (which the Examiner alleges as corresponding to the gate junction (PMOS) M55/M56 of Park) and to connect a second capacitor as taught by Wu between the second common node and the

output node (which the Examiner alleges as corresponding to the gate junction M51/M52 (NMOS) of Park). Since Wu specifically discloses the first and second capacitors to be connected between NMOS transistors, as seen in Fig. 3 of Wu, Applicant submits that the Examiner's combination of the Applicant's prior art and Park with that of Wu does not disclose or suggest the recited features of claim 3.

For at least the reasons submitted above, we would submit that claim 3 is patentable.

Claims 6 and 8, which depend from claim 3, are patentable at least by virtue of their dependencies.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

/ S. Stuart Lee /

S. Stuart Lee
Registration No. 61,124

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860
WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: October 9, 2009